IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of

Huilong Zhu et al.

Serial No.: 10/708,378

Filed: February 27, 2004

Conf. No.: 2377

Group Art Unit: No.: 2818

Examiner: N. Ngo

For: HYBRID SOI/BULK SEMICONDUCTOR TRANSISTORS

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

AMENDED APPELLANT'S BRIEF UNDER 37 C.F.R. §41.37 IN RESPONSE TO NOTICE OF NON-COMPLIANT APPEAL BRIEF

This amended brief is in furtherance of the Notice of Appeal, filed in this case on December 11, 2006, with a Pre-Appeal Brief Request for Review; a Decision on which was mailed January 22, 2007. An Appellants Brief on Appeal was filed March 22, 2007, with a petition for a one-month extension of time. This amended brief is being filed in response to a Notice of Non-Compliant Appeal Brief mailed May 16, 2007, indicating that the Summary of Claimed Subject Matter did not include a mapping to the specification. This amended brief is identical to the brief filed March 22, 2007, but for amendment of that section and supplying sub-headings in regard to the arguments made in regard to dependent claims, together with reasons that claims discussed under a given sub-heading should not stand or fall together. And a summary of the arguments presented therein as a concluding paragraph.

This amended brief contains these items under the following headings, and in the order set forth below (37 C.F.R. §41.37(c)):

I. REAL PARTY IN INTEREST

II. RELATED APPEALS AND INTERFERENCES

III. STATUS OF CLAIMS

IV. STATUS OF AMENDMENTS

V. SUMMARY OF CLAIMED SUBJECT MATTER

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

VII. ARGUMENTS

- ☐ ARGUMENT VIIA. REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH
- ☐ ARGUMENT VIIB. REJECTIONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH
- ☑ ARGUMENT VIIC. REJECTIONS UNDER 35 U.S.C. §102
- ☑ ARGUMENT VIID. REJECTIONS UNDER 35 U.S.C. §103
- ☐ ARGUMENT VIIE. REJECTION OTHER THAN 35 U.S.C. §§102, 103 AND 112

VIII. CLAIMS APPENDIX

IX. EVIDENCE APPENDIX

X. RELATED PROCEEDINGS APPENDIX

I. Real Party in Interest

The real party in interest in the appeal is:

☐ the party named in the caption of this brief.

☑ the following party:

International Business Machines Corporation of Armonk, New York

II. RELATED APPEALS AND INTERFERENCES

With respect to other appeals, interferences or judicial proceedings that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal:

☑ there are no related appeals, interferences or judicial proceedings related to, which directly affect or may be directly affected by or have a bearing on the Board's decision in this pending Appeal.

☐ these are as follows:

III. STATUS OF CLAIMS

The status of the claims in this application are:

A. Total number of claims in Application

Claims in the application are: 1 - 15 and 21 - 25

B. Status of all the claims:

1. Claims cancelled: 16 - 20
2. Claims withdrawn from consideration but not cancelled: None
3. Claims pending: 1 - 15 and 21 - 25
4. Claims allowed: 6 - 9 and 12 - 14
5. Claims rejected: 1 - 5, 10 - 11, 15 and 21 - 25

C. Claims on Appeal.

The claims on appeal are: 1 - 5, 10 - 11, 15 and 21 - 25

IV. STATUS OF AMENDMENTS

The status of amendments filed subsequent to the final rejection are as follows:

The amendment under 37 C.F.R. §1.116 filed November 9, 2006 has been or should have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention as defined in the claims on appeal including independent claims 1, 11 and 21, is directed to a transistor structure, shown in a generalized form in Figure 1; particular embodiments of which are illustrated in Figures 8, 19 and 25B. (Claims 1 and 21 are directed to a field-effect transistor, *per se*, while claim 11 is directed to an integrated circuit containing a field-effect transistor recited in terms otherwise identical to claim 1.) Such transistors, as recited in claims 1 and 11, include a layer of material (e.g. 12) within the substrate 10 wherein the layer of material includes a discontinuity 18 aligned to the gate structure G. Particularly since it is contemplated to be preferable to form such a transistor at very small size, the accuracy of alignment of the discontinuity 18 and the gate G is relatively sensitive to position or "overlay" errors and alignment of the discontinuity to the gate structure as recited in all independent claims 1, 11 and 21 (or self-alignment - claims 2 and 22) of the discontinuity 18 to the gate G (e.g. "having a discontinuity [18] aligned to said gate structure [G]" (claims 1 and 11) or "having a discontinuity which includes an edge [i.e. corresponding to an edge of void 170' in Figure 14] which is located in a position defined by an edge said gate structure [as shown, for example, in Figures 3 and 8 or 14 - 15 and described in paragraphs [0022] and [0025] and paragraph [0028], respectively" (claim 21)) is considered to be much preferred and an important feature of the claimed invention since overlay errors can thus be avoided (see, for example, paragraph 0022) as well as allowing the invention to be applied to a wide variety of transistor designs and materials (e.g. the three disclosed preferred embodiments of Figures 2 - 8 (described at paragraphs [0022] - [0026]), 9 - 19 (described at paragraphs [0027] - [0033] and 20 - 25B (described at paragraphs [0034] - [0039], respectively, which also contain descriptions of the achievement of alignment of the discontinuity to the gate structure). Likewise the layer of material in which the discontinuity is defined may include a shaped (e.g. of "staircase" cross-section)

feature at the discontinuity to limit the conduction channel depth (as might also be achieved using a more expensive semiconductor on insulator (SOI) or ultra-thin SOI (UT-SOI) wafer or substrate while allowing control of effective semiconductor layer thickness and formation of (possibly silicided) recessed source and drain structures of arbitrary depth for reduced resistance without requiring resort to raised source and drain structures which cause deleterious increase of overlap capacitance and consequent compromise of transistor performance.

The discontinuity which is aligned to the gate G of the transistor, as recited in claims 1, 11 and 21 and disclosed as discussed above, can serve several purposes such as providing a conduction path 18 to the channel region of the transistor to avoid floating body effects characteristic of transistors formed on SOI substrates for limitation of conduction channel depth (see claim 21), to allow formation of a further gate structure below the conduction channel and/or to apply stress directly to the conduction channel region of the transistor (see claim 21) in order to adjust carrier mobility without causing warping of the substrate as discussed, for example, in paragraphs 0018 and 0019.

Dependent claims 2 and 22 recite self-alignment of the discontinuity to the transistor gate, claims 3, 4, 23 and 24 recite that the film in which the discontinuity is formed is a stressed film, claims 5 and 25 recite that the film in which the discontinuity is defined is an insulating film and claims 10 and 15 recite inclusion of a void (e.g. 260 of Figure 25A - see paragraphs 0036 and 0037) within the layer of semiconductor material.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on Appeal are:

1.) the rejection of claims 1 - 5, 11 and 21 - 25 under 35 U.S.C. §102 as being anticipated by Krivokapic et al.; and

2.) the rejection of claims 10 and 15 under 35 U.S.C. §103 as being unpatentable over Krivokapic et al. in view of Bae.

ARGUMENT VIIA. REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH

There are no grounds of rejection under 35 U.S.C. §112, first paragraph.

ARGUMENT VIIB. REJECTIONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH

There are no grounds of rejection under 35 U.S.C. §112, second paragraph.

ARGUMENT VIIC. REJECTIONS UNDER 35 U.S.C. §102

Claims 1 - 5, 11 and 21 - 25 have been rejected under 35 U.S.C. §102 as being anticipated by Krivokapic et al. Krivokapic et al. teaches a transistor having an oxide layer 30 with an opening 28 therein and having an epitaxial layer 32 grown in the opening 28 and above the oxide layer 30 which is covered by a gate oxide 34. The gate of the transistor of Krivokapic et al. is formed by depositing nickel spacers 38 adjacent isolation structures (and far from the opening 28) with amorphous silicon between the spacers. A nickel silicide gate electrode is then formed centrally and aligned with the opening between the isolation structures by recrystallization (see column 2, lines 51 - 59).

As has been previously argued, *nothing remotely involving layer 30 or opening 28* in Krivokapic et al. is aligned to the gate structure 42 but, on the contrary, the gate structure 42 is aligned (by a particular and evidently critical metallurgical process) to the *opening between isolation structures 24* as explicitly stated at column 2, lines 53 - 55, and at most, indirectly to the opening 28. This structure is for the explicitly recited purpose of controlling the formation of a silicided gate structure consistent with formation of silicided source and drain structures 64 (which are *raised* structures inherently exhibiting increased overlap capacitance, as noted in paragraph 0004 of the specification, which the invention avoids as discussed, *inter alia*, in paragraph 0019 of the specification) . The only contemplated function of opening 28 is for a body contact (see column 1, lines 20 - 28) for which alignment is not critical. There is no discussion in Krivokapic et al. of limiting channel depth or applying stress to the transistor channel for enhancing carrier mobility.

Thus, Krivokapic et al. does not answer the claim recitation of "a discontinuous film of material within said layer of semiconductor material and *having a discontinuity aligned to said gate structure*" (claims 1 and 11, emphasis added) or "said discontinuous film having a discontinuity *which includes an edge which is*

located in a position defined by an edge said gate structure (claim 21, emphasis added) much less the recitation of "said discontinuity defining a structure for performing at least one of:

defining a depth of a conduction channel of said field effect transistor within said layer of semiconductor material to less than said predetermined distance from said surface of said semiconductor material; and

applying stress to said conduction channel of said field effect transistor" as further recited in claim 21 or self-alignment of the discontinuity with the gate structure as recited in claims 2 and 22 or a stressed film as recited in claims 3 - 4 and 23 - 24 which support meritorious advantages of the present invention which are not available from or suggested or even contemplated by Krivokapic et al. Accordingly, Krivokapic et al. does not anticipate any of claims 1 - 5, 11 or 21 - 25 as the Examiner appears to recognize.

Nevertheless, the Examiner continues to insist that the claims are "product by process" claims since, as illustrated in Figure 5a and 6 of Krivokapic et al., the opening 28 and the gate electrode 42 appear to be generally aligned with each other. However, it is respectfully submitted that the recitations of "a discontinuity aligned to said gate structure" in claims 1 and 11 and "a discontinuity which includes an edge which is located in a position defined by an edge said gate structure" in claim 21 are clearly structural recitations and not process recitations and that the "product by process analysis is wholly unwarranted and does not justify ignoring explicit recitations of the claims as the Examiner has done.

Further, it is respectfully submitted that even if a product by process analysis were warranted, such an analysis merely shifts the burden of proof to Applicant to demonstrate differences between the invention and the structure disclosed in the reference which Applicant has, in fact, repeatedly done. Specifically, the present invention, by providing for alignment of the discontinuity to the gate structure,

supports the meritorious functions of:

1.) correct and accurate alignment of the gate and the discontinuity is guaranteed in the invention whereas, in Krivokapic et al. it is not and the alignment is only approximate and provided in an indirect manner which increases the likelihood of misalignment;

2.) even if the gate structure of Krivokapic is located in the correct position, there appears to be no mechanism in Krivokapic et al. for accurately controlling the geometry of the edges of the resulting gate structure as provided by the invention and, in fact, gate 42 is depicted in Krivokapic et al. as being irregular in shape in Figures 5a and 5b;

3.) the invention can be applied to any transistor design and transistor manufacturing process including SOI and bulk semiconductor devices whereas the process required in Krivokapic et al. appears to limit design flexibility, particularly in regard to source and drain structure geometry and does not appear to be capable of being scaled to small sizes and the film discontinuity cannot be sub-lithographic is dimensions as can be achieved by the present invention provides, and

4.) the invention provides a structure which can be formed of virtually any semiconductor material whereas Krivokapic et al. relies on very specific metallurgy and does not teach, suggest or even recognize a need for adjustment of carrier mobility by stressing of the channel, if such an effect is even possible since, in Krivokapic et al., the channel 34 must be epitaxially grown over the film 30. Accordingly, it is respectfully submitted that Applicant has met the burden of clearly demonstrating differences of the claimed invention from the structure of Krivokapic et al. to shift the burden of demonstrating anticipation back to the Examiner; which burden the Examiner has not and apparently cannot answer since none of the above-enumerated meritorious effects are even contemplated by Krivokapic et al.

Argument VIIC(1), Claims 2 and 22

As discussed above, Krivokapic et al. not only fails to teach or suggest alignment of the discontinuity with the gate structure as recited in the independent claims of this application, but fails to teach or suggest achieving such alignment by self-alignment as recited in claims 2 and 22, which allows process simplification with increased manufacturing yield. Self-alignment is utterly inconsistent with the structure and manufacturing methodology of Krivokapic et al. It is also respectfully submitted that claims 2 and 22 do not stand or fall together since they depend from different independent claims

Argument VIIC(2) Claims 3, 4, 23 and 24

Additionally, in regard to claims 3 and 4, the Examiner has asserted that the film 30 of Krivokapic et al. can inherently be a stressed film (as also recited in claims 23 and 24 which the Examiner does not mention and which, it is respectfully submitted, do not stand or fall together with claims 3 and 4 since they depend from different independent claims). For inherency to be shown in a rejection for anticipation, it is well-established that the characteristic which is not disclosed but asserted to be inherent must *necessarily and unavoidably* follow from subject matter which is, in fact, disclosed in the reference relied upon which is clearly not the case and essentially admitted to be an improper assertion of inherency by the language used by the Examiner: "*can* inherently *be* a stressed film. Such an improper assertion of inherency is respectfully submitted to be an admission of lack of anticipation of these claims by Krivokapic et al. and a clear attempt to supplement the inadequacy of Krivokapic et al. to answer explicit claim recitations with subject matter disclosed in the present application.

Accordingly, it is respectfully submitted that the rejection of claims 1 - 5, 11 and 21 - 25 for anticipation by Krivokapic is clearly in error and untenable.

Therefore, reversal of the Examiner in regard to this ground of rejection is clearly believed to be in order and such action is respectfully requested.

ARGUMENT VIID. REJECTIONS UNDER 35 U.S.C. §103

Claims 10 and 15 have been rejected under 35 U.S.C. §103 as being unpatentable over Krivokapic et al. in view of Bae; the Examiner admitting that Krivokapic et al. does not teach or suggest provision of a void within the layer of semiconductor material and relying on Bae for teaching the provision of void 35. The Examiner does not rely on Bae for mitigation of any of the deficiencies of Krivokapic et al. or justifying the ignoring of explicit claim recitations or assertion of inherency as discussed above in Argument VIIC. Moreover, the Examiner asserts that the provision of a void is for the purpose of suppressing floating body effects which is clearly incorrect since the void 35 is formed wholly within an insulating layer. (The reduction of floating body effects is clearly disclosed to be achieved by porous silicon 23b at column 4, lines 29 - 30.) Rather, as disclosed at column 4, lines 36 - 43, the voids 35 form a silicon on air (SOA) structure to reduce capacitance since air has a lower dielectric constant than oxide forming the remainder of layer 33a.

While such a function of reducing capacitance may be desirable in Krivokapic et al., the disclosed technique of forming the voids (e.g. undercutting the transistor source and drain regions from isolation structure locations as illustrated in Figure 6 followed by oxidation and deposition of insulator as described in column 5, lines 31 - 52) appears to be utterly inconsistent with the process disclosed in Krivokapic et al. et al. where isolation structures are required from the earliest stages of fabrication. It is well-established that it is improper to propose a modification of a reference structure which would preclude operation of the reference in the intended manner (see, for example, In re Gordon, 221 USPQ 1125 (Fed. Circ., 1984)). Therefore, it is respectfully submitted that the combination of teachings and modification of Krivokapic et al. proposed by the Examiner is improper and, moreover, clearly an exercise in attempted hindsight reconstruction of the invention based on the present disclosure.

More importantly, however, Bae teaches the provision of voids in an isolation structure formed of insulating material. Therefore, even if the combination of Bae with Krivokapic et al. were to be considered proper, that combination does not answer the recitation of "a void *within said layer of semiconductor material*" as recited in claims 10 and 15 (emphasis added). This recitation is significant since the void as provided by the invention allows regulation of the thickness and location of a stressed film; a meritorious effect not taught or suggested by Bae (or Krivokapic et al.) and is also thus seen to constitute an improper reliance upon hindsight.

Thus, in summary, this ground of rejection is clearly in error and improper since the combination of Krivokapic et al. and Bae does not answer the recitations of alignment of a film discontinuity with a gate structure as recited in the independent claims from which claims 10 and 15 depend or the recitations of a void in the semiconductor layer explicitly recited in claims 10 and 15 as well as being an improper combination of references and evidencing application of impermissible hindsight. Accordingly, it is respectfully submitted that reversal of the Examiner's position in regard to the rejection of claims 10 and 15 as being unpatentable over Krivokapic et al. in view of Bae is in order and such action is respectfully requested.

ARGUMENT VIIE. REJECTION OTHER THAN 35 U.S.C. §§102, 103 AND 112

There are no grounds of rejection other than under 35 U.S.C. §102 and §103.

VIII. CLAIMS APPENDIX

The text of the claims involved in the appeal are:

1. A field effect transistor formed at a surface of a layer of semiconductor material, said field effect transistor comprising

a gate structure formed on said surface of said layer of semiconductor material, and

a discontinuous film of material within said layer of semiconductor material and having a discontinuity aligned to said gate structure.

2. A field effect transistor as recited in claim 1, wherein said discontinuity is self-aligned to said gate structure.

3. A field effect transistor as recited in claim 1, wherein said discontinuous film is a stressed film

4. A field effect transistor as recited in claim 3, wherein said stressed film comprises an insulator.

5. A field effect transistor as recited in claim 1, wherein said discontinuous film comprises an insulator.

10. A field effect transistor as recited in claim 1, further including a void within said layer of semiconductor material.

11. An integrated circuit including a field effect transistor formed at a surface of a layer of semiconductor material, said field effect transistor comprising

a gate structure formed on said surface of said layer of semiconductor material, and

a discontinuous film of material within said layer of semiconductor material and having a discontinuity aligned to said gate structure.

15. An integrated circuit as recited in claim 11, further including a void within said layer of semiconductor material.

21. A field effect transistor formed at a surface of a layer of semiconductor material, said field effect transistor comprising

a gate structure formed on said surface of said layer of semiconductor material, and

a discontinuous film of material within said layer of semiconductor material at a predetermined distance from said surface of said layer of semiconductor material, said discontinuous film having a discontinuity which includes an edge which is located in a position defined by an edge said gate structure,

said discontinuity defining a structure for performing at least one of:

defining a depth of a conduction channel of said field effect transistor within said layer of semiconductor material to less than said predetermined distance from said surface of said semiconductor material; and

applying stress to said conduction channel of said field effect transistor.

22. A field effect transistor as recited in claim 21, wherein said discontinuity is self-aligned to said gate structure.

23. A field effect transistor as recited in claim 21, wherein said discontinuous film is a stressed film

24. A field effect transistor as recited in claim 23, wherein said stressed film comprises an insulator.

25. A field effect transistor as recited in claim 21, wherein said discontinuous film comprises an insulator.

IX. Evidence Appendix

No additional evidence is relied upon in this Appeal.

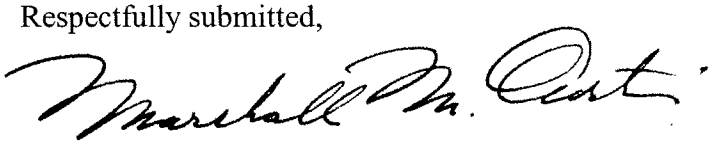
X. RELATED PROCEEDINGS APPENDIX

There are no other proceedings related to this Appeal.

Conclusion

For the reasons set forth above, it is respectfully submitted that the claims clearly define the invention in regard to features which are not taught, suggested or within the purview of the level of ordinary skill of the art as determinable from the evidence thereof provided by the prior art relied upon. No *prima facie* demonstration of anticipation or obviousness of any claim has been made and the asserted grounds of rejection are clearly seen to be in error and untenable. The insufficiency of the prior art relied upon to support such conclusions is underscored by the improper assertions of product-by-process analysis and inherency as discussed above. Accordingly, reversal of the Examiner's position in regard to the asserted grounds of rejection is respectfully submitted to be in order and such action is respectfully requested.

Respectfully submitted,



Marshall M. Curtis
Reg. No. 33,138

Whitham, Curtis & Christofferson, P.C.
11491 Sunset Hills Road, Suite 340
Reston, VA 20190
Tel. (703) 787-9400
Fax. (703) 787-7557
Customer No. 30743